IN THE SPECIFICATION:

Page 3, line 30, please insert the following paragraph:

Figure 3 schematically shows components of the high speed interface type semiconductor memory device in accordance with embodiments of the invention.

Page 5, lines 10-13, please replace the paragraph as shown:

Figure 2 illustrates an internal structure of the DRAM of the high speed interface type semiconductor memory device in accordance with the present invention, especially an internal structure of a quadruple ~~date~~ data rate SDRAM.

Page 6, line 29 through page 7, line 9, please replace the paragraph as shown:

The write operation of the quadruple ~~date~~ data rate SDRAM will now be described. When receiving a data synchronized with the clock signal CCLK and a write command from the controller 100, the DRAM generates the first internal clock and clock bar signals wclk, wclkb delay locked by the DLL unit 10, and the second internal clock and clock bar signals wclk90, wclk90b. Thereafter, the DRAM respectively latches write data passing through the DQ pad and the input buffer BF5 according to the first internal clock and clock bar signals wclk, wclkb and the second internal clock and clock bar signals wclk90, wclk90b. Here, the latched data are transmitted to a write driver through an internal I/O bus, and stored in cells of a memory array. The n-th DRAM and the other DRAMs 1~n-1 perform different read operations.

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